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Review Article

Flexible Smart Display with Integrated Graphics Rasterizor using Single Grain TFTs

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Abstract

Flexible electronics is a fast emerging market and includes electronics fabricated on flexible substrates, large area displays, low cost and disposable electronics. Both research and commercial institutions around the world have been trying to develop low temperature processes which will enable fabrication of electronic devices on arbitrary substrates including glass and plastic. While most of these technologies are still in the research phase, many approaches have shown promising results. One such technology is being developed in DIMES, TU Delft which uses single grain silicon crystals to fabricate Single Grain Thin Film Transistors (SG-TFTs) at plastic compatible temperatures. SG-TFTs and other similar technologies can potentially enable fabricating electronics directly on arbitrary substrates. This would further enable integration of embedded intelligence in devices that would enhance the current functionalists of displays. This paper is an effort in this direction as it undertakes a study to design a flexible display with an integrated graphics rasterizor unit. The paper introduces the novel idea to move parts of the graphics pipeline from the CPU/GPU to the display. This will add intelligence to the display so as to realize a smart-display. The paper proposes several architectures for implementing a rasterizor unit on smart-display, conceptually fabricated on a flexible substrate using SG-TFT technology. While the transistors fabricated with SG-TFT and similar technologies are relatively slower than the standard CMOS, this paper proposes and concludes that a tile based system design can potentially result into enhanced system performance.

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INTRODUCTION

It is estimated that the overall panel display market will continue to grow to a potential worth of 100 billion by the year 2015. The focus will be upon larger and higher-resolution displays for TV, multimedia, computer and portable applications, as shown in the figure 1. Flexible displays will clearly gain a larger share of this market in the future.

Flexible Display Technologies Overview

One of the primary technologies used for manufacturing flexible displays utilizes organic semiconductor materials. An Organic Light Emitting Diode (OLED) is an electroluminescent device containing organic thin films with amorphous structures. Due to the amorphous characteristics, fabrication of OLED on large substrates is possible. OLED deposition is a low process temperature and hence it can be deposited on flexible substrates as well.

The use of silicon for producing flexible displays has been limited to the use of amorphous and poly Silicon in fabricating Thin Film Transistors (TFTs) used for active-matrix addressing circuits. In order to integrate various kinds of functions, such as gate and data drivers, data storage, processing unit and wireless communication unit on a flexible plastic substrate, TFTs need to have electron mobility of more than 500 cm2/Vs (Ryoichi Ishihara *et al*., 2010). A Single Grain TFT (SG-TFT) is a transistor that is

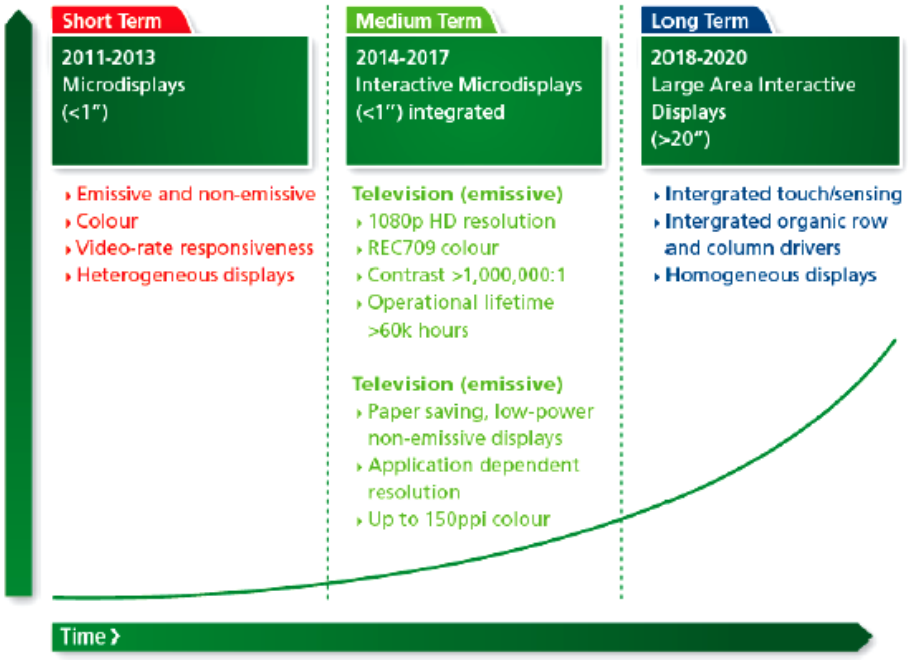

Figure 1: Expected display functionalities with market growth.

fabricated inside a single grain of silicon, as shown in the figure 2. At DIMES, Delft University of Technology, SG-TFTs fabricated by the micro-Czochralski process show highly competitive performance with features such as an electron field-electron mobility of 600 cm2/Vs, a hole mobility of 250 cm2/Vs, an offset current of few pico-amperes and a sub threshold slope of about 200 mV/dec (Ryoichi Ishihara *et al*., 2010).

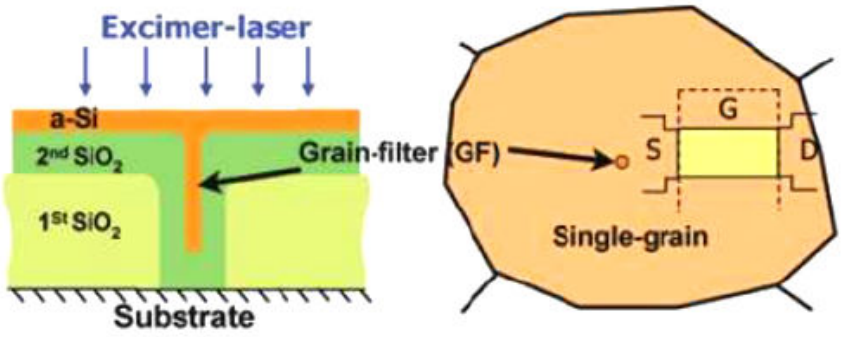

Figure 2: Schematic of u-Czochralski (grain-filter) process (left) and single-grain Si TFTs (right) (Ryoichi Ishihara *et al*., 2010).

Designing a Smart-Display

The growing commercial interest in designing such flexible displays with enhanced functionalities poses many interesting research questions, especially from an embedded system's design perspective. For instance:

a) What would be the overall system architecture of these flexible displays?

b) Would the system architecture be just an adaptation of the current display architectures on a new hardware platform?

c) Could data processing and storage be done in a different way utilizing the benefits of direct fabrication of electronics on flexible substrates?

d) Could certain processing and/or memory be moved from the current Central Processing Unit (CPU) and shifted to the flexible display? And if so, how much processing can be shifted?

e) What would be the impact on total power, speed and hardware used in the newarchitecture?

f) Can new features be integrated that would enhance the existing functionalists ofa typical display?

This paper focuses on designing display architecture with an integrated rasterization unit. SG-TFT technology is used as the reference fabrication technology on a flexible substrate. Rasterization based graphics pipeline is conceptually divided into two stages and the rasterization stage is shifted to the flexible display. This embedding of logic and memory on the display provides additional intelligence to the display unit due to which it is referred to as a smart-display in the paper.

Display Graphics Rendering Methods

In computer graphics, a 3D scene from the real-life is reproduced on a 2D display screen. The method for computing such an image is called rendering. It is the process of generating an image from a model by means of computer programs. A scene-file contains objects in a strictly defined language or data structure, for instance it would contain geometry, viewpoint, texture, lighting, and shading information as a description of the virtual scene. The data contained in the scene is passed to a rendering program to be processed which produces an output digital image that could then be shown to the user on a 2D screen. There are two primary methods of graphics rendering that are used in the contemporary systems. They are:

1. Rasterization based rendering.
2. Ray Tracing based rendering.

After comparing a conceptual design of both these methods, the following conclusions were drawn:

1. The time taken for the serial fragment processing operations and the digital to analog conversion is well within the required time for displaying a video to the user.
2. Rasterization stage can be moved to the smart-display with the CPU/GPU sending3D triangle information to the smart-display as it will reduce the amount of data processing required by the smart-display.

Based on these conclusions, the rasterization stage is shifted to the smart-display and several possible implementation architectures are proposed in the next sections of the paper.

Rasterization Architectures on the Smart-Display

3D ICs (Yuan Xie *et al.*, 2009) are being considered as attractive options for overcoming the barriers in interconnect scaling and thereby offering another opportunity to continue performance improvements in ICs. 3D integration technologies offer many advantages for designing ICs. These include (Yuan Xie *et al.*, 2009):

1. Reduction in interconnect wire length, which results in improved performance and reduced power consumption.
2. Improved memory bandwidth by stacking memory on multiple cores with Through Silicon Vias (TSV) connections between the layers.
3. Support for heterogeneous integration which results in novel architectures to fabricate analog, digital and memory elements in a system.
4. Smaller form factor which results in higher packing density and smaller foot-print due to the addition of a third dimension to the conventional two dimensional layout
5. Potential lower cost design.

3D ICs can be used for increasing the System-On-Panel (SoP) functionalities. There are different approaches to 3D IC integration including package level, wafer level and device level integration. However, vertical stacking of electronics at the device level or monolithic integration gives the largest decrease in interconnect length and highest density of interconnects between the stacked layers. Such a monolithic stacking of electronic devices has been demonstrated by the SG-TFT technology (Mohammad Reza *et al*., 2009) as demonstrated in Figure 3 which allows denser packaging of hardware elements.

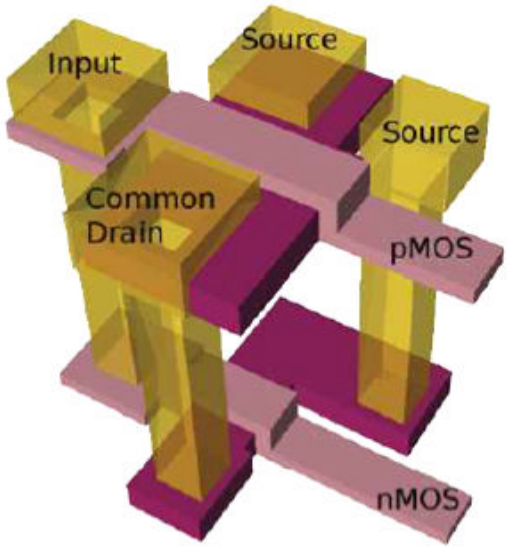

Figure 3: The schematics of a 3D inverter with a pMOS on the top and an nMOS on the bottom layer.

Embedded System Architectures for Streaming Multimedia

While designing the streaming media based embedded system for smart-display the following overall system design principles are considered:

1. Appropriate algorithms are selected.
2. Processing elements are matched to the algorithms.
3. Pipelining and/or Parallelism techniques are utilized wherever efficiently supported by the selected algorithms.
4. 3D integration technologies are considered to fabricate logic and memory.

As depicted in the figure 4 splitting the graphics pipeline and implementing the rasterization unit on smart-display will result in the following overall system architecture:

1. The CPU/GPU will execute the Application Stage of the OpenGL graphics pipeline and will transform the geometric primitives into triangles.
2. Each vertex of the triangle contains information pertaining to its corresponding location, color and depth.
3. The CPU/GPU will transmit these triangle data to the smart-display
4. The smart-display will process this incoming triangle information.
5. The smart-display will rasterize each triangle into its corresponding pixel values and will display the final image to the user.

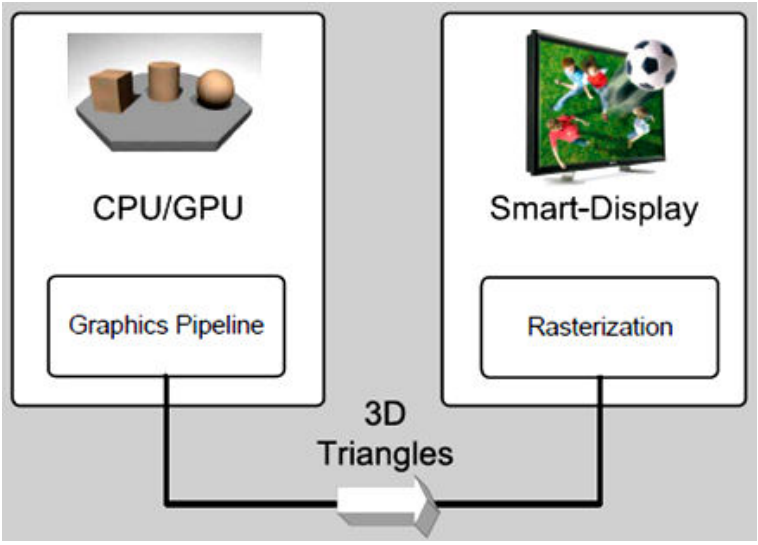

Figure 4: Basic Architecture of Smart-Display

This architecture will result into the following changes in the current system:

1. The graphics pipeline is now split with an expected output of 3D triangles instead of frame buffer data. This will decrease the workload on the CPU/GPU.
2. An overhead is added to the CPU/GPU to pack and transmit the triangle information and for the smart-display to receive and unpack this information. A suitable protocol needs to be implemented between CPU/GPU and smart-display for this purpose.
3. The transmitted data over CPU/GPU-Smart Display interface is now 3D triangle information instead of framebuffer data which will result in less bandwidth support required by the interface. This will also reduce the overall system power consumption from the data transmission perspective.
4. The smart-display will process only the triangle data and not the entire fram ebuffer data. This reduces the functional complexity required to be supported by the smart-display.
5. The smart-display can utilize several architectures to implement rasterization of triangle data to further improve the system performance.

The 3D integration technologies as described in Section 4.1 provide a design space in which the functional requirements of the smart-display can be partitioned in a multilayered design fabricated behind the display. This design space allows multiple architectural properties. As demonstrated in figure 5 multiple layers could be used for integrating analog, digital and memory elements behind the OLED layer on the smart-display.

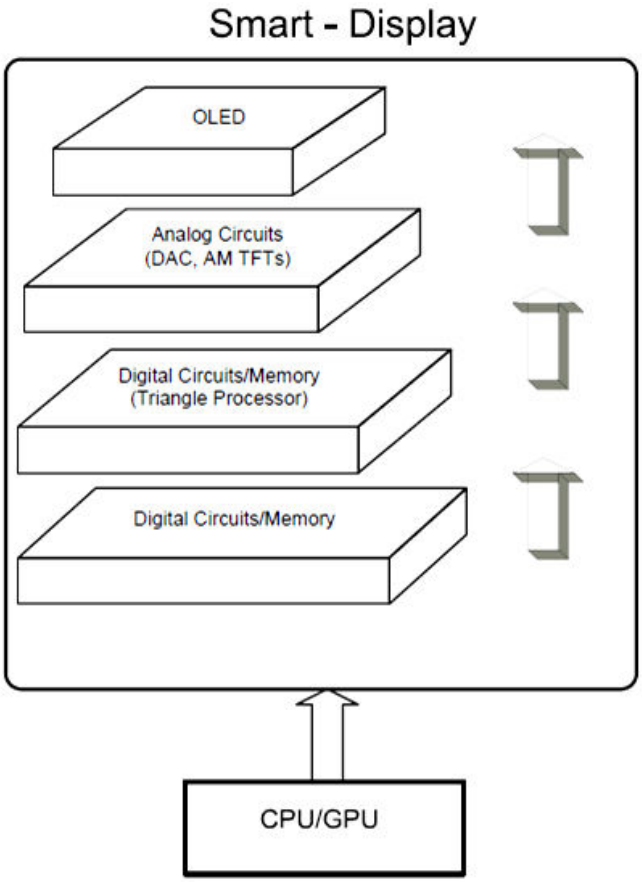

Figure 5: 3D Design partitioning Possibilities for Smart-Display.

Smart-Display Architecture

On such 3D architectures, there are many ways in which rasterization operations can be carried out by the smart-display. For instance:

1. All the triangle processing could be performed by a single core.

2. Each incoming triangle can be completely rasterized in a single stage before processing the next triangle
3. A set of triangles can be rasterized together in an independent processing core while the incoming triangles are stored in a shared memory by another independent processing core.
4. The triangle processing could be split into multiple stages and different cores can implement the pipelining stages.
5. Within any core the data processing could be further pipelined.
6. The pixel memory could be interfaced to the triangle processor using a direct connection to each pixel or all the pixels could be interfaced as one giant addressable memory unit.
7. A tile based architecture can be used wherein which each tile will be responsible for rasterizing the triangles that are covered within the tile boundary.
8. The pixels can be interconnected by a network and triangle processor can interface the pixels using this network.

After analyzing several similar possible architectures, tile based architecture was found most suitable for smart display. As depicted in the figure 6, it has the following characteristics:

1. The triangle processor layer is divided into multiple units called tiles, as shown in Figure1.6 with each tile responsible for performing rasterizing operations pertaining to their corresponding pixels.
2. Each incoming triangle is processed by a triangle dispatcher module that is fabricated at the center of the triangle processing layer.
3. For each incoming triangle, the triangle dispatcher calculates the potential tiles the intersect with the triangle
4. The dispatcher then sends the triangle information to each potential tile using the two possible interconnects.
5. After receiving a new triangle each tile calculates which pixels covered under the tile are inside the triangle.
6. For all the pixels covered inside the triangle, the final color is calculated if the new z value is greater than the current. The current z value is read from the corresponding pixel memory.
7. Each tile is directly connected to all the pixels covered under it using vertical interconnects and hence each tile transfers the new calculated values using this direct connection to specific pixels.

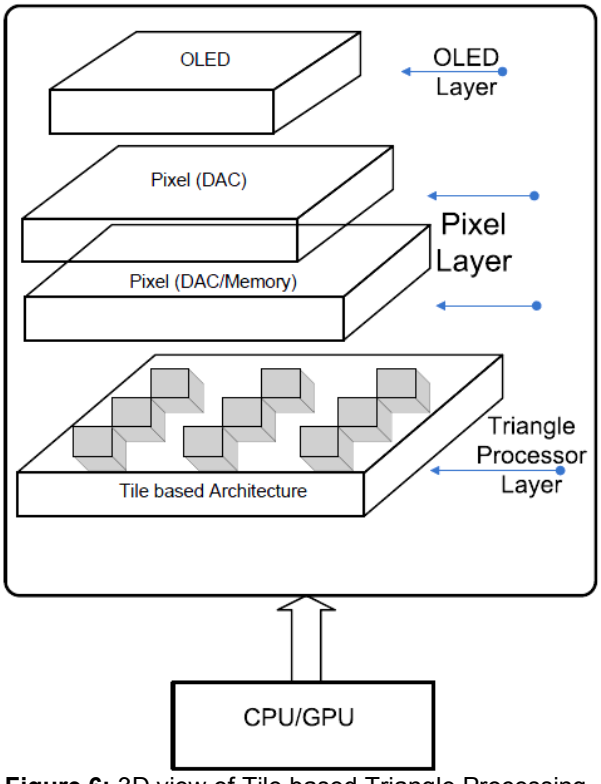

Figure 6: 3D view of Tile based Triangle Processing.

This architecture has the following merits:

1. All the tiles can carry out their expected operations independent of each other. This adds parallelism to the system which significantly improves the overall rasterization speed.
2. The triangle dispatcher module requires simple hardware and can be advantageously located at the center of the triangle layer.

This architecture has the following demerits:

1. The entire triangle information needs to be sent to each tile by the triangle dispatcher which increases the internal data traffic.
2. Each tile needs to perform a check for all the pixels in the tile if they are covered by the triangle.
3. Each tile needs to be taking care of the worst case scenario of incoming triangle data traffic which increases the amount of overall hardware required by the smart display.

The figure 1.7 below depicts a front view of the architecture

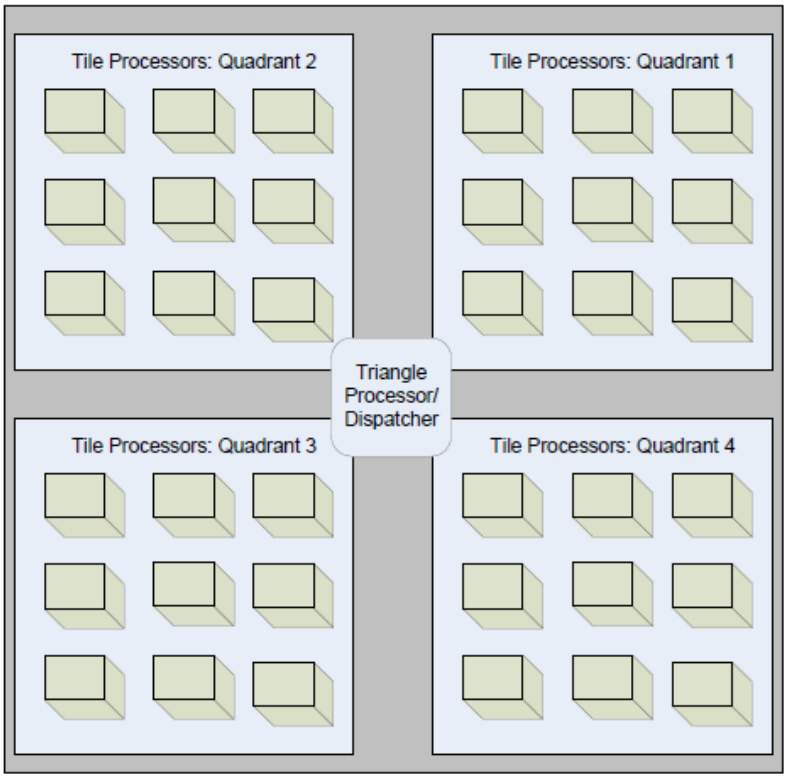

Figure 7: Tile based Architecture for Smart-Display.

SG-TFT Technology Constraints

In order to support the 3D layered design architectures, certain constraints are imposed by the SG-TFT technology. These constraints place practical restrictions on the integration of logic and memory elements behind the different layers. As a result, some of the design considerations discussed so far can be potentially unfeasible to realize using the current state of the SG-TFT technology.

Fabrication Area under one OLED Pixel

The number of SG-TFTs that could be used for realizing the processing and storage elements depend on the designed layout of the electrical circuits as well as design choices for smart-display. In order to find the minimum number of TFTs that can be fabricated under an OLED pixel, an empirical calculation is performed as follows:

1. Area of one pixel = 300X300 microns (Amir Naeimi *et al*., 2011)
2. Area of one SG-TFT=12X12 microns (Alessandro Baiano *et al*., 2009)
3. Minimum spacing between each TFT=1 micron

Total TFTs under one pixel (single substrate) = (300 x 300) /(13 x 13) = 532 TFTs.

As monolithic stacking of devices is demonstrated by SG-TFT technology in (Mohammad Reza *et al*., 2009), twolayers are used for each pixel. Hence the total number of TFTs available for each pixelis approximately 1000.

8 bit Integrated DAC for one Pixel

A Digital to Analog Converter (DAC) is required by each pixel of the smart-display. Pixels with integrated DAC have been a strong feature in the Liquid Crystal on Silicon (LCOS) (Hoon-Ju-Chungnd *et al*., 2008) based micro displays industry where dense integration of electronics devices is carried out using CMOS technology. For direct view displays including laptops and TV screens, recently LTPS (Low Temperature Poly Silicon) (Tae-Wook Kim *et al*., 2008) have been used to realize novel integrated pixel designs. In (Tae-Wook Kim *et al*., 2008), the authors fabricate an 8 bit DAC using LTPS method with 2 micron as the minimum feature size. As shown in Figure 1.8 together with the timing signal generator the total area occupied by this 8 bit DAC is 960 x 82 = 78,720 microns.

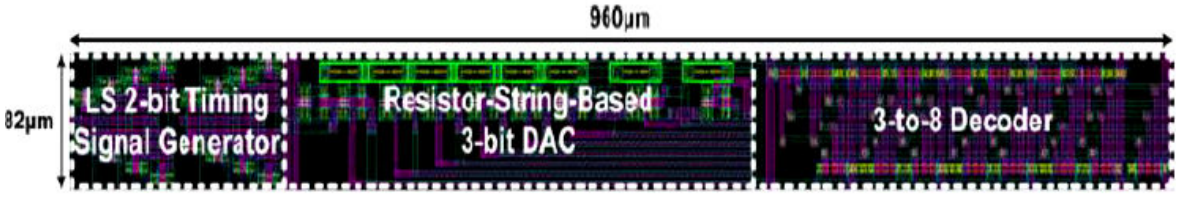

Figure 8: LTPS based 8 bit DAC Area (Tae-Wook Kim *et al*., 2008).

Ten bytes of DRAM for one Pixel

Since the total available area behind each pixel is (300 x 300) microns for one layer (Amir Naeimi *et al*., 2011) and the 8 bit integrated DAC occupies 78,720 microns 4.8.2, 10 bytes of Dynamic Random Memory (DRAM) along with 5 sense amplifiers required by the smart- display can be integrated in the OLED pixel in two (300 x 300) layers. In DRAM, dynamic refers to the need to periodically refresh DRAM cells so that they can continue to retain the stored bit. This requires a sense amplifier (Bihju Chiu *et al*., 1998). The main function of asense amplifier is to sense or detect stored data from a selected memory cell. As shown in the figure 4, a typical sense amplifier consists of 3 NMOS and 3 PMOS transistors and one sense amplifier is required for each data line of the DRAM memory.

Since each SG-TFT is of an average size of 13 microns each DRAM cell occupies an area of 20 micron square. This means a total area of 1600 micron square for 10 bytes of DRAM. As for a sense amplifier, a total of 60 transistors are required for each pixel that covers an approximate fabrication area of 780 micron square. Therefore 10 bytes of DRAM cells along with an integrated sense amplifier occupies an area of 2380 micron square. This empirical calculation suggests that is feasible to fabricate an 8 bit DAC, 10 bytes of DRAM and 5 sense amplifiers on two layers behind an OLED pixel using SG-TFT technology.

Impact of SG-TFT Technology Constraints

SG-TFT technology constraints restrict the design space for the amount of processing elements that could be placed in each layer in the smart-display and hence restrict certain aspects of the proposed architectures in this chapter. With these constraints hardware architecture as demonstrated in Figure 9 seems the most feasible for smart-display.

This architecture has the following characteristics:

1. The pixel-layer consists of 2 layers. The 8 bit DAC, TFTs for Active matrix addressing and 10 DRAM bytes is fabricated on these two layers.
2. Triangle processing is implemented one layer behind the pixel-layer.
3. Proposed architectures 1, 2 and 3 can be potentially designed using SG-TFT technology.

Architecture Simulation and Results

A POSIX C based platform is chosen for performing software simulations to design the system architectures proposed in the previous section. The simulation platform is designed to have a flexible configuration for simulating multiple ways in which data processing and storage elements could be integrated in the smart-display.

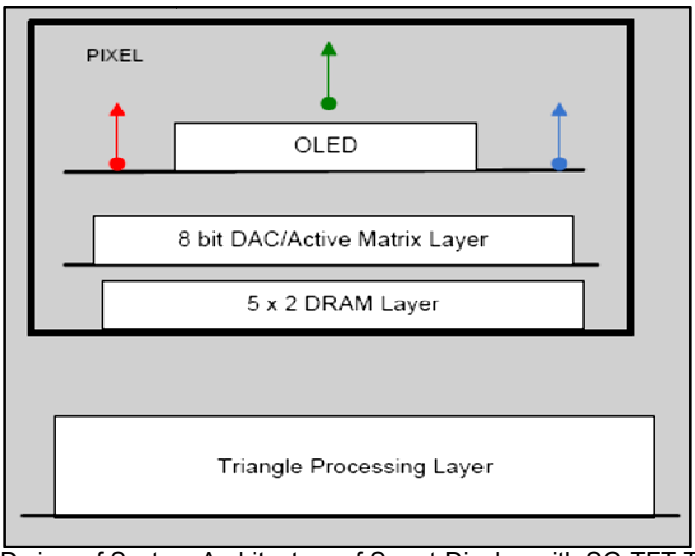

Figure 9: 3D view of System Architecture of Smart-Display with SG-TFT Technology.

The following process is undertaken for simulating the proposed architecture:

1. The triangle processor module utilizes single threads to calculate the number of tiles an incoming triangle potentially touches using a bounding-box method for the tiles.
2. Along with the triangle data, the bounding-box information is transmitted to atriangle dispatcher module that works as a different thread.
3. The triangle dispatcher module utilizes an SDL timer callback function module and simulates the functionality of transmitting the incoming triangle packets based on the bounding box information using either the row/column interface module or the network interface module.
4. After receiving a triangle packet, each Tile performs rasterization operation in a single thread and updates the pixel.
5. The total trace is measured at the input of the triangle dispatcher module and each tile.
6. The overall time taken by the tiles to rasterize all the triangles for the three chosen pixel resolutions are measured utilizing 16 or 25 SDL timer callback functions depending on the configured tile-size.

The graph in figure 10 depicts the measured time for rasterization by the proposed architecture for the two chosen tile sizes. The following inferences are drawn from this graph:

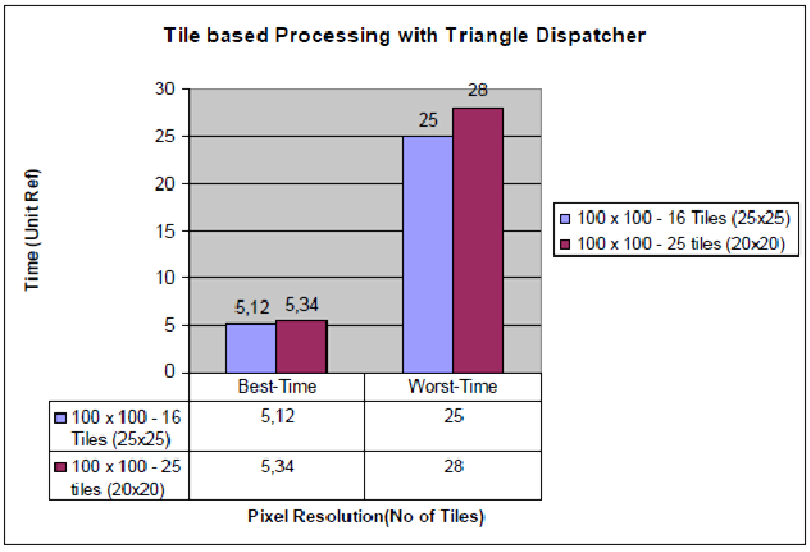

Figure 10: Tile based processing with triangle dispatcher: Timing simulation measurements.

CONCLUSION

To improve the execution speed and add parallelism to the systema tile based system architecture is proposed in this paper. In this architecture, the pixels are divided into a certain number of units called tiles such that each tile is independently responsible for rasterizing their corresponding pixels. A triangle dispatcher unit is utilized which performs a bounding box test for each tile and transfers the incoming triangles to the potential tiles that touch the triangle. Each tile then rasterizes the pixels that are covered under the tile and send the final color values to the pixels. While this architecture further improves the execution speed of rasterization process, it does require more hardware.

The choice of the most suitable architecture for smart-display depends on various factors including speed, energy and overall cost of the system. Considering the relative speed of the SG-TFT technology with respect to CMOS, speed of the system is perhaps the most important parameter. Based on the merits and demerits of the proposed architectures as well as the observed simulation results, overall the tile based architecture is found to be the most suitable architecture for smart-display. Based on the simulation analysis, the tile based architecture is found to be the most suitable for designing rasterization unit on smart-display with SG-TFT technology.

The main contributions and conclusions of this paper can be summarized as follows:

- A rasterization based graphics pipeline offers a simple hardware structure compared to ray tracing for implementing smart-display.
- A serial implementation of the selected steps in Fragment Processing using SG-TFT technology can be executed within sufficient time to display a video at a rate of 25 frames/second.
- A rasterization module can be implemented on the smart-display. This reduces the incoming data-rate to the display as only 3D triangle information needs to be sent by CPU/GPU instead of frame buffer data.
- A tile based architecture provides the best execution time and least traffic forrasterization on smart-display.
- Overall, the tile based architecture is the most suitable one for implementing rasterization on the smart-display.

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